

**WHAT IS CLAIMED IS:**

- 1     1.     A boundary-scan device to a macro, comprising:  
2             a plurality of signal paths connected to the macro, each having  
3     a data signal input end and a data signal output end for signal  
4     transmission during normal mode operations; and  
5             a plurality of circuitries for said plurality of signal paths,  
6     respectively, each having capability of capturing a signal transmission  
7     event that a signal has past through one of said plurality of signal  
8     paths during test mode operations.
  
- 1     2.     The boundary-scan device as claimed in claim 1, wherein each  
2     of said plurality of circuitries includes a gate having an input coupled to  
3     said data signal output end of one of said signal paths, and a scan cell  
4     having a capturing input coupled to an output of said gate.
  
- 1     3.     The boundary-scan device as claimed in claim 1, wherein each  
2     of said plurality of circuitries includes a gate having an input coupled to  
3     said data signal output end of one of said signal paths, and two scan  
4     cells of different types, each having a capturing input coupled to an  
5     output of said gate.
  
- 1     4.     The boundary-scan device as claimed in claim 2,  
2             wherein each of said plurality of circuitries includes a selector  
3     having an output coupled to said data signal output end of one of said  
4     plurality of signal paths, a first input coupled to said data signal input  
5     end of said one signal path, and a second input coupled to said scan  
6     cell for said one signal path, and  
7             wherein said plurality of circuitries include a selector controlling  
8     logic unit,  
9             said selector controlling logic unit enabling each of said  
10    selectors to connect the first input thereof to the output thereof during  
11    normal mode operations,  
12            said selector controlling logic unit enabling each of selected

13 ones of said selectors to connect the first input thereof to the output  
14 thereof and enabling each of non-selected ones of said selectors to  
15 connect the second input thereof to the output thereof during test  
16 mode operations.

1 5. The boundary-scan device as claimed in claim 4, wherein said  
2 selector controlling logic unit includes a plurality of first logic elements,  
3 each controlling one of said selected ones of said selectors, and a  
4 plurality of second logic elements, each controlling one of said  
5 non-selected ones of said selectors.

1 6. The boundary-scan device as claimed in claim 4, wherein said  
2 selector controlling logic unit includes a first logic element controlling  
3 each of said selected ones of said selectors, and a second logic  
4 element controlling each of said non-selected ones of said selectors.

1 7. The boundary-scan device as claimed in claim 3,  
2 wherein each of said plurality of circuitries includes a selector  
3 having an output coupled to said data signal output end of one of said  
4 plurality of signal paths, a first input coupled to said data signal input  
5 end of said one signal path, and a second input,  
6 said second input of each of said selectors being coupled to one  
7 of said two scan cells for said one signal path, and  
8 wherein said plurality of circuitries include a selector controlling  
9 logic unit,  
10 said selector controlling logic unit enabling each of said  
11 selectors to connect the first input thereof to the output thereof during  
12 normal mode operations,  
13 said selector controlling logic unit enabling each of selected  
14 ones of said selectors to connect the first input thereof to the output  
15 thereof and enabling each of non-selected ones of said selectors to  
16 connect the second input thereof to the output thereof during test  
17 mode operations.

1 8. The boundary-scan device as claimed in claim 7, wherein said  
2 selector controlling logic unit includes a plurality of first logic elements,  
3 each controlling one of said selected ones of said selectors, and a  
4 plurality of second logic elements, each controlling one of said  
5 non-selected ones of said selectors.

1 9. The boundary-scan device as claimed in claim 7, wherein said  
2 selector controlling logic unit includes a first logic element controlling  
3 each of said selected ones of said selectors, and a second logic  
4 element controlling each of said non-selected ones of said selectors

1 10. The boundary-scan device as claimed in claim 1, wherein each  
2 of said plurality of signal paths and one of said plurality of circuitries  
3 form one of a plurality of boundary scan cells.

1 11. The boundary-scan device as claimed in claim 10,  
2 wherein said plurality of boundary scan cells include:  
3 a plurality of input boundary scan cells, each being coupled, at  
4 said signal data input end thereof, to one of a plurality of output pins of  
5 a peripheral circuit and, at said signal data output end thereof, to one  
6 of a plurality of input pins of the macro; and  
7 a plurality of output boundary scan cells, each being coupled, at  
8 said signal data input end thereof, to one of a plurality of output pins of  
9 the macro and, at said signal data output end thereof, to one of a  
10 plurality of input pins of the peripheral circuit,  
11 wherein each of said plurality of input boundary scan cells  
12 allows signal transmission through said signal path thereof from said  
13 signal data input end to said signal data output end when the  
14 peripheral circuit is a device under test during test mode operations,  
15 wherein each of said plurality of output boundary scan cells  
16 allows signal transmission through said signal path thereof from said  
17 signal data input end to said signal data output end when the macro is  
18 a device under test during test mode operations.

1 12. The boundary-scan device as claimed in claim 11,  
2 wherein each of said plurality of input boundary scan cells  
3 includes an input-side gate having an input coupled to said data signal  
4 output end thereof;

5 wherein said plurality of input boundary scan cells include a  
6 plurality of scan cells, respectively, which are interconnected to form  
7 an input-side portion of a scan chain;

8 wherein, during test mode operations, said plurality of scan  
9 cells of said input-side portion of said scan chain are operative to  
10 capture gate outputs of said input-side gates, respectively, for shifting  
11 each of said captured gate outputs through said scan chain;

12 wherein, during test mode operations, said plurality of scan  
13 cells of said input-side portion of said scan chain are operative to  
14 update outputs, respectively;

15 wherein each of said plurality of input boundary scan cells  
16 includes an input-side selector having a first input coupled to one of  
17 said signal data input ends and a second input coupled to one of said  
18 plurality of scan cells of said input-side portion of said scan chain;

19 wherein, when the peripheral circuit is a device under test  
20 during test mode operations, each of said input-side selectors selects  
21 a signal on one of said data signal input ends to appear on the mating  
22 one of said data signal output ends;

23 wherein each of said plurality of output boundary scan cells  
24 includes an output-side gate having an input coupled to said data  
25 signal output end thereof;

26 wherein said plurality of output boundary scan cells include a  
27 plurality of scan cells, respectively, which are interconnected to form  
28 an output-side portion of said scan chain;

29 wherein, during test mode operations, said plurality of scan  
30 cells of said output-side portion of said scan chain are operative to  
31 capture gate outputs of said output-side gates, respectively, for  
32 shifting each of said captured gate outputs through said scan chain;

33 wherein, during test mode operations, said plurality of scan  
34 cells of said output-side portion of said scan chain are operative to

35 update outputs, respectively;  
36 wherein each of said plurality of output boundary scan cells  
37 includes an output-side selector having a first input coupled to one of  
38 said data signal input ends and a second input receiving said updated  
39 output; and  
40 wherein, when the macro is a device under test during test  
41 mode operations, each of said output-side selectors selects a signal on  
42 one of said data signal input ends to appear on the mating one of said  
43 data signal output ends.

1 13. The boundary-scan device as claimed in claim 10, wherein each  
2 of said plurality of boundary scan cells is coupled to one of pins of the  
3 macro and allows signal transmission from said data signal input end  
4 thereof to said data signal output end thereof for the signal to be  
5 captured.

1 14. The boundary-scan device as claimed in claim 13,  
2 wherein each of said plurality of output boundary scan cells  
3 includes a gate having an input coupled to said data signal output end  
4 thereof;

5 wherein said plurality of boundary scan cells include a plurality  
6 of scan cells, respectively, which are interconnected to form a scan  
7 chain;

8 wherein, during test mode operations, said plurality of scan  
9 cells of said scan chain are operative to capture gate outputs of said  
10 gates, respectively, for shifting each of said captured gate outputs  
11 through said scan chain;

12 wherein, during test mode operations, said plurality of scan  
13 cells of said output-side portion of said scan chain are operative to  
14 update outputs, respectively;

15 wherein each of said plurality of boundary scan cells includes a  
16 selector having a first input coupled to one of said data signal input  
17 ends and a second input receiving said updated output; and

18 wherein a test control signal indicating a device under test

19 during test mode operations causes selected one of said selectors to  
20 select a signal on one of said data signal input ends to appear on the  
21 mating one of said data signal output ends.

1 15. The boundary-scan device as claimed in claim 12,  
2 wherein each said plurality of boundary scan cells includes a  
3 first scan cell of the first type and a second scan cell of the second  
4 type; and  
5 wherein said first scan cells are interconnected form a first scan  
6 chain for shifting captured data from one to another of said first scan  
7 cells and updating outputs, and said second scan cells are connected  
8 serially one after another to form a second scan chain for shifting  
9 captured data from one to another of said second scan cells.

1 16. The boundary-scan device as claimed in claim 14,  
2 wherein each said plurality of boundary scan cells includes a  
3 first scan cell of the first type and a second scan cell of the second  
4 type; and  
5 wherein said first scan cells are interconnected to form a first  
6 scan chain for shifting captured data from one to another of said first  
7 scan cells and updating outputs, and said second scan cells are  
8 connected serially one after another to form a second scan chain for  
9 shifting captured data from one to another of said second scan cells.

1 17. The boundary-scan device as claimed in claim 12, wherein,  
2 during normal mode operations, each of said selectors selects a signal  
3 on one of said data signal input ends to appear on the mating one of  
4 said data signal output ends.

1 18. The boundary-scan device as claimed in claim 14, wherein,  
2 during normal mode operations, each of said selectors selects a signal  
3 on one of said data signal input ends to appear on the mating one of  
4 said data signal output ends.

1 19. The boundary-scan device as claimed in claim 15, wherein,  
2 during normal mode operations, each of said selectors selects a signal  
3 on one of said data signal input ends to appear on the mating one of  
4 said data signal output ends.

1 20. The boundary-scan device as claimed in claim 16, wherein,  
2 during normal mode operations, each of said selectors selects a signal  
3 on one of said data signal input ends to appear on the mating one of  
4 said data signal output ends.